AD-A031 302 HARRY DIAMOND LABS ADELPHI MD F/G 9/2
INVESTIGATION OF LONG-TERM STORAGE AND REVERSE LINK METHODS FOR--ETC(U)
AUG 76 T MANOLATOS
UNCLASSIFIED HDL-TM-76-20 NL

1 OF 1
ADA031302

END

DATE
FILMED
11 -76

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER HDL-TM-76-20	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Investigation of Long-Term Storage and Reverse Link Methods for the 5-Inch SALGP Data Link		5. TYPE OF REPORT & PERIOD COVERED Technical Memorandum 6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) Telemachos Manolatos		8. CONTRACT OR GRANT NUMBER(s) MIPR: N60921-76-MP-RD035
9. PERFORMING ORGANIZATION NAME AND ADDRESS Harry Diamond Laboratories 2800 Powder Mill Road Adelphi, MD 20783		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS El Code: Navy
11. CONTROLLING OFFICE NAME AND ADDRESS Naval Surface Weapons Center White Oak Silver Spring, MD 20910		12. REPORT DATE Aug [redacted] 76 13. NUMBER OF PAGES 13
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) HDL-437644		15. SECURITY CLASS (of this report) Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

DRCMS Code: 693000.12.11560

HDL Project: 437644

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Remote set
Guided projectile
5-inch guided projectile

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The 5-in. guided projectile must be programmed with certain flight data prior to launch. These data must be stored in the projectile for up to 5 min without power connections. Two methods of accomplishing this are discussed: (1) A nonvolatile metal nitride oxide silicon memory and (2) a complementary metal oxide semiconductor memory driven by energy stored on a capacitor. It is also desirable to check the accuracy of the

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE 1 UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

163050

message sent. A method of reading the message back by varying the impedance of the secondary coil is discussed.

CONTENTS

FIGURES

TABLES

1. INTRODUCTION

This study augments the 5-in. Guided Projectile Remote Set Proposal submitted by the Harry Diamond Laboratories (HDL) on 21 May 1975. Since this proposal was submitted, the Naval Surface Weapons Center, Dahlgren, VA, provided funds for HDL to investigate two system characteristics that were not considered in the original proposal: (1) a means of storing the message in the projectile for up to 5 min prior to firing and (2) a reverse data link by which the receiving circuitry in the projectile could positively respond, indicating that it received a correct message. In considering methods of adding these features, it was assumed that the system requirements listed in table I would also be met.

This paper discusses two methods for 5-min data storage. The first is a volatile complementary metal oxide semiconductor (CMOS) memory powered by a capacitor and the second, a nonvolatile metal nitride oxide silicon (MNOS) memory. A method for incorporating the reverse link was devised and tested. The last section of this report describes the rationale for selecting the proposed memory and reverse link system and its impact on the total system.

TABLE I. SYSTEM REQUIREMENTS

Characteristics	Values
Operating temperature	-40 to 70°C
Stored bits	22
Total time to set	1.3 s
Time setting	
Max time to function	50 s
Setting increment	1 s
Accuracy	0.1% of max time

2. FIVE-MINUTE STORAGE

2.1 The CMOS Memory

The CMOS memory must be powered during the 5-min storage time. One method used to provide stored energy is in a capacitor charged by the carrier signal of the setter during the time a set message is sent. This method requires that the current drain on the capacitor be minimized, done by turning off all circuitry, except the memory, once the message is sent. The drain then consists of the quiescent current required for the memory and various leakage currents that must exist.

The drain on the capacitor is very small. At room temperature, with typical leakage currents, the capacitor could drive the CMOS for hours. Under extreme conditions of temperature and atypical (but within specification) leakage currents, the drain becomes significant and must be calculated.

Figure 1 illustrates a power supply configuration that can drive all of the circuitry during a message and then turn off all but the memory. While the setter is on, the memory is powered through CR4. The remaining logic is powered through CR4 and the MOS field effect transistor (FET), Q_1, which is turned on whenever battery or coil voltage is present. When battery or coil voltage is not present, Q_1 is off, CR4 is back biased, and the capacitor drives only the CMOS memory. During this time, this circuit reduces to the leakage model shown in figure 2. The reverse leakage current of CR4, Q_1, and the Zener diode, CR6, are modeled as current sources, while the leakage of the capacitor and the quiescent current are simulated with resistors. The instantaneous voltage across the capacitor, V(t), is

$$V(t) = \left(V_o + IR\right)e^{-t/RC} - IR ,$$

where V_o = initial voltage on the capacitor. Solving for time, t, and setting V(t) equal to the minimum operating voltage for the CMOS, V_{min}, yields

$$t_s = -RC \ In\left(\frac{V_{min} + IR}{V_o + IR}\right) .$$

This is the time it takes the capacitor to discharge to the point where it can no longer support the memory.

Table II shows leakage currents that can exist in specific devices used in this design. Using the maximum leakage that could occur at 70°C, an initial voltage of 13 V, and V_{min} = 3 V yields t_s = 7.9 s. This is far from acceptable. Most of the current drain is due to the high leakage specifications for the Zener diode and the RCA CD4006AD shift registers. These specifications are well above the typical values expected and include almost the entire distribution of devices. By selecting a lower leakage level, which would result in approximately a 50-percent yield, the leakage currents in the last column of table II may be obtained. By use of these values, t_s = 4 min, 50 s. By use of the conservative model and the fact that five components must exhibit worst-case behavior, the storage time requirement is essentially met.

In summary, the CMOS memory can store the data for 5 min, if three components (one Zener diode, two shift registers) are selected for minimum leakage currents.

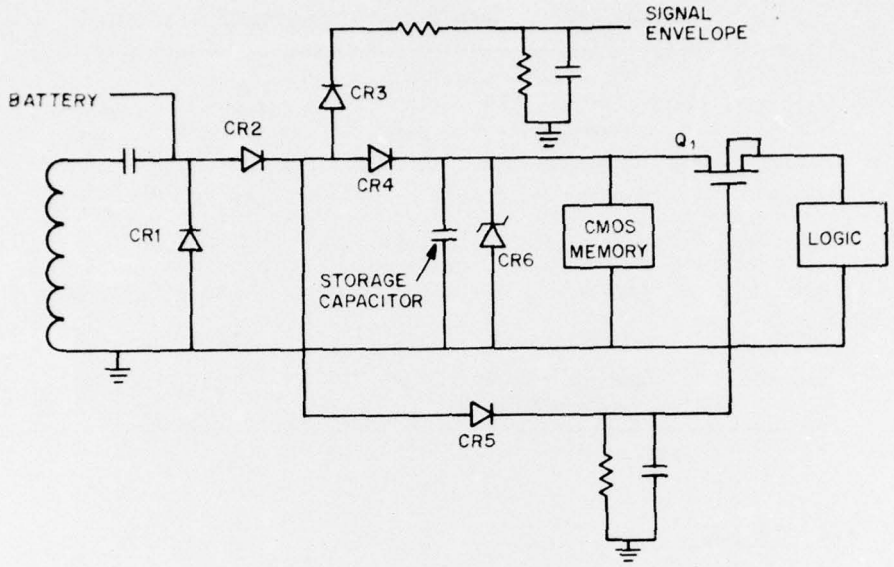

Figure 1. Power supply for CMOS memory.

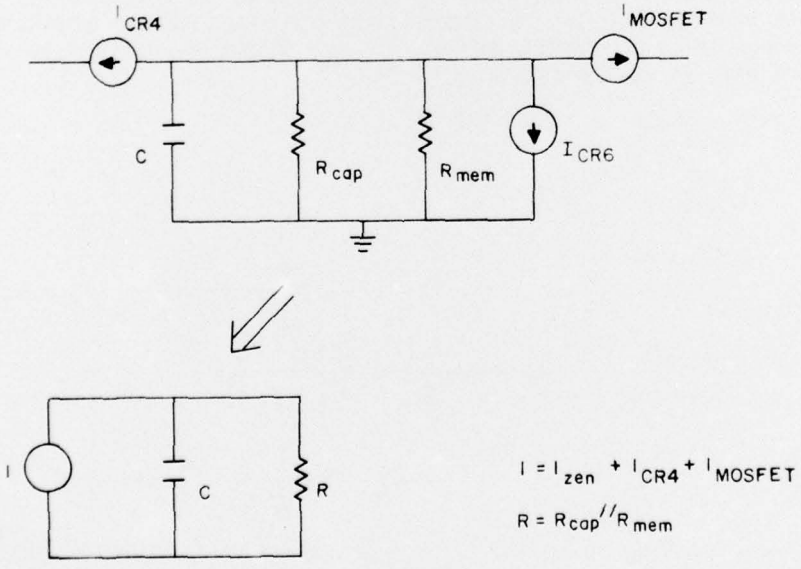

Figure 2. Leakage model for CMOS memory.

TABLE II. LEAKAGE CURRENTS FOR CMOS MEMORY

Part	Example	Model	Max leakage at 70°C (A)	Leakage at 70°C (select*) (A)
Zener	IN4736	I	100	0.1*
Shift register	CD4006AD	R	16 at 5 V	0.3 at 5 V*
FET	ZN4351	I	0.25 μ	0.25 μ
Diode	IN4448	I	0.5 μ	0.5 μ
Capacitor	Sprague (120 μF) 1090127X0015CFO	R	5 μ at 15 V	5 μ at 15 V

2.2 The MNOS

Another method of storing the data is to use an MNOS memory. This is a nonvolatile memory that requires no power to retain the message. An MNOS memory cell is shown in figure 3. The gate threshold voltage is programmed by large gate-to-substrate voltages (V_{GS}). A positive V_{GS} causes a high threshold voltage, while a negative V_{GS} causes a low thresheld voltage. The value of the threshold is retained if power is interrupted. The memory cell is read by applying a gate voltage between the two possible threshold voltages. If the transistor turns on, it may be defined as a "1"; if it remains off, it is defined as a "0."

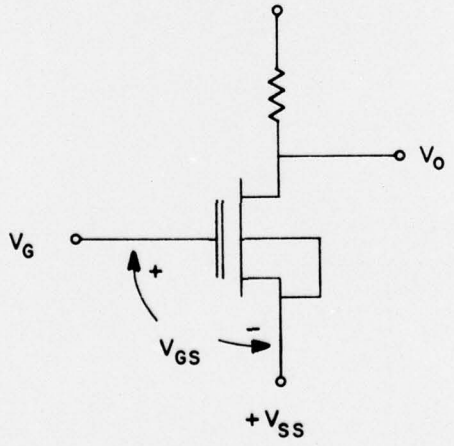

Figure 3. The MNOS memory cell.

The time required to set the threshold is approximately 10 ms with an amplitude of 25 V. In normal practice, the entire memory is erased; then the "1" states are set in parallel. The entire erase-write cycle would then take about 20 ms. Figure 4 shows the block diagram for an MNOS memory system.

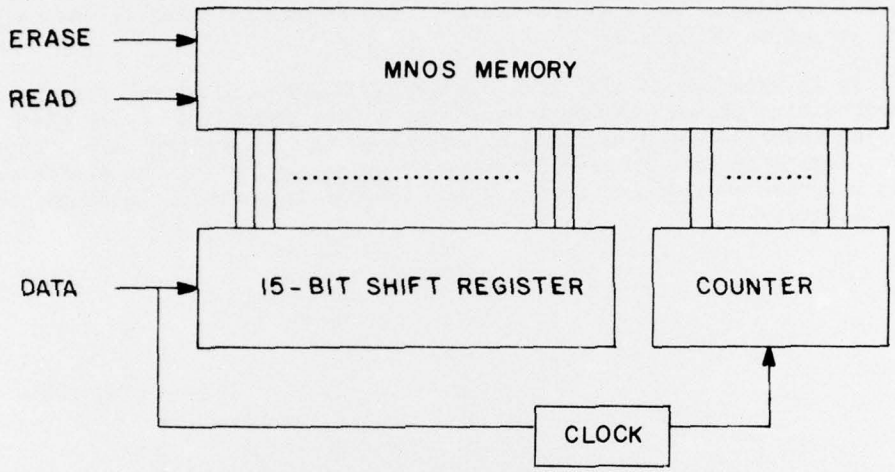

Figure 4. The MNOS memory.

The mode and code data are clocked into the 15-bit shift register, and an analog window allows the counter to index for a time proportional to the desired set time. During the serial data transfer, the MNOS memory is erased. Following the analog window, when data transfer is complete, a 10-ms read pulse loads the memory. The data are now stored regardless of power supply voltage.

Several characteristics of this system should be noted. First, although the programming pulses have a relatively high amplitude and long duration, only two are required at a very low current level (nanoamperes). This means very little total energy must be transferred to the receiver. Second, the MNOS circuitry is more complex than that of the CMOS memory because it adds an MNOS memory. Also, a means of steering the proper programming and read voltages to the gate of each bit must be added.

3. REVERSE DATA LINK

It is desirable to have a positive response from the projectile electronics indicating a message has been received and the message is accurate. This reverse link can be established as follows. By shorting and unshorting the receiving coil while the transmitting coil is on, the amplitude of the transmitted signal may be modulated. This occurs because

the changing impedance of the secondary coil is reflected to the primary coil. Thus, a reverse link can be established by amplitude modulation of the transmit signal.

The feasibility of this concept was demonstrated in the laboratory with the circuit shown in figure 5. The primary coil was approximately 5 in. in diam while the secondary coil was 3 in. in diam and approximately 6 in. away. An adequate signal amplitude of 250 mV was detected at the output and can easily be processed.

It is recommended that the entire message should be repeated during the reverse link phase. Although some type of bit count and parity check with a yes-no response would probably be adequate, the circuitry on the projectile required to do this is more than that required to return the entire message. The returned message can be compared with the transmitted message to check for accuracy.

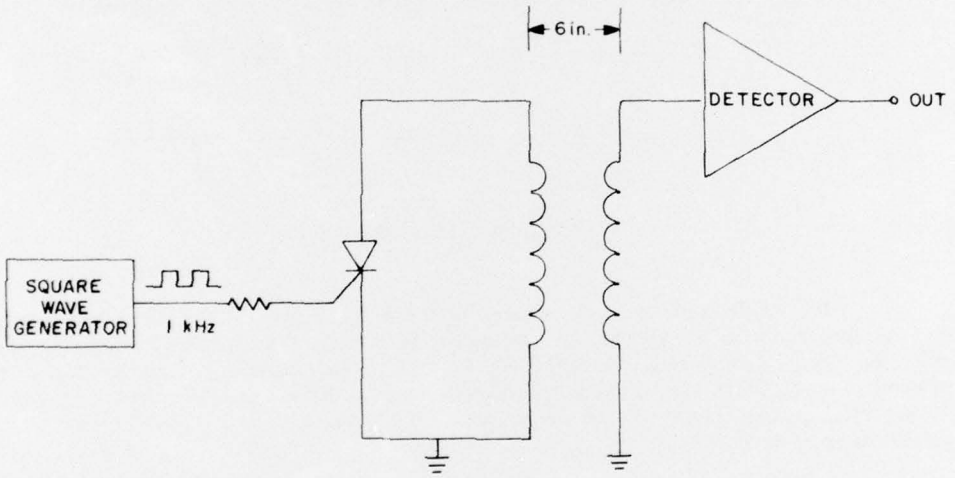

Figure 5. Reverse link laboratory simulation.

4. RECOMMENDED SYSTEM

4.1 Selection of Memory

Table III is a comparison of the CMOS and MNOS memories. The CMOS is preferable in all categories except risk in coil design. The 120-μF storage capacitor must be charged within approximately 500 ms to allow enough time to set the message. This means a relatively high current must be generated in the receiving coil. The data suggest that this charging can be done, but it has not yet been demonstrated.

TABLE III. CMOS VERSUS MNOS

Characteristic	CMOS	MNOS
Power required	High current, low voltage	Very low current, high voltage
Receiver circuit complexity	Medium	High
Coil design risk	Medium	Low
Circuit design risk	Low	Medium
Cost	Low	Medium
Ability to increase storage time	Poor	Excellent

Because the CMOS memory is desirable from every other aspect, use of the CMOS storage is recommended. Primary emphasis should be placed on demonstrating the ability to charge the storage capacitor in a reasonable time. Otherwise, the MNOS memory would serve as a backup approach.

4.2 System Description

A block diagram of the recommended receiver is shown in figure 6. The timing diagram for the system is given in figure 7. A continuous signal is sent for at least 500 ms, which charges the power-supply capacitor. This is followed by a 10-ms reset pulse, which initializes all the circuitry. Then, 15 bits of data are encoded on a pulse-width-modulated signal and are shifted into the CMOS memory. These pulses are followed by two timing pulses separated by the function time divided by 1024. A counter in the receiver begins counting on the first pulse and stops on the second pulse. The final count is proportional to the desired function time. This count is also shifted to the CMOS memory. With the CMOS storage register in a ring counter configuration, the data set is shifted through the output flip-flop once. The serial output of the shift register is then applied to the silicon controlled rectifier (SCR) gate, thus returning the message to the setter. If the message is acceptable to the setter, nothing further happens. However, if the message is incorrect, the cycle begins again at the reset pulse.

The prototype would be designed with integrated circuits available off the shelf. For the CMOS memory, this means about 6 $in.^2$ of circuit board. A multilayer board (three or four layers) would also be required. If the MNOS memory is used, approximately a 9-$in.^2$ board area is required.

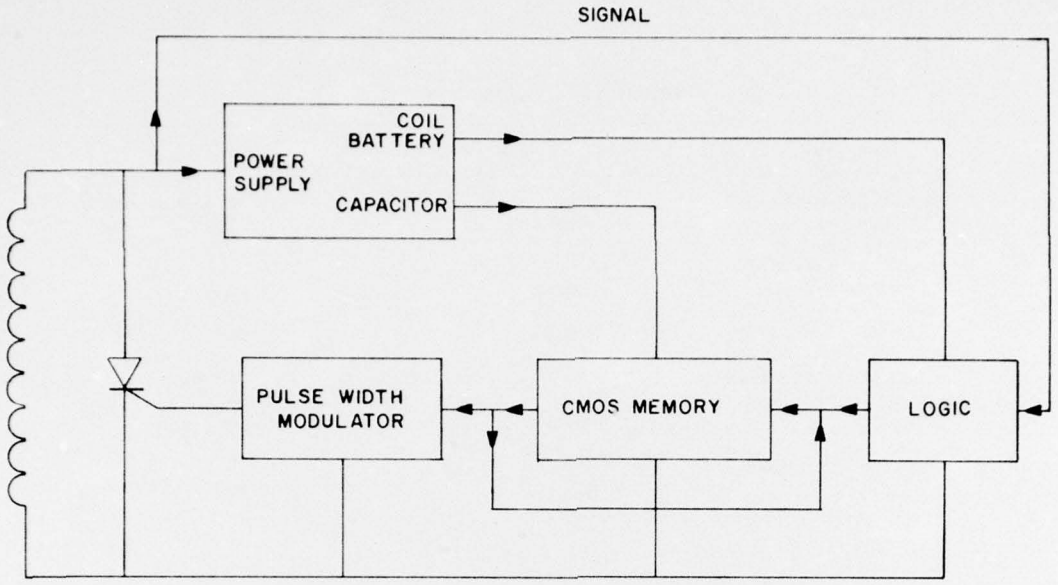

Figure 6. Remote set with CMOS memory.

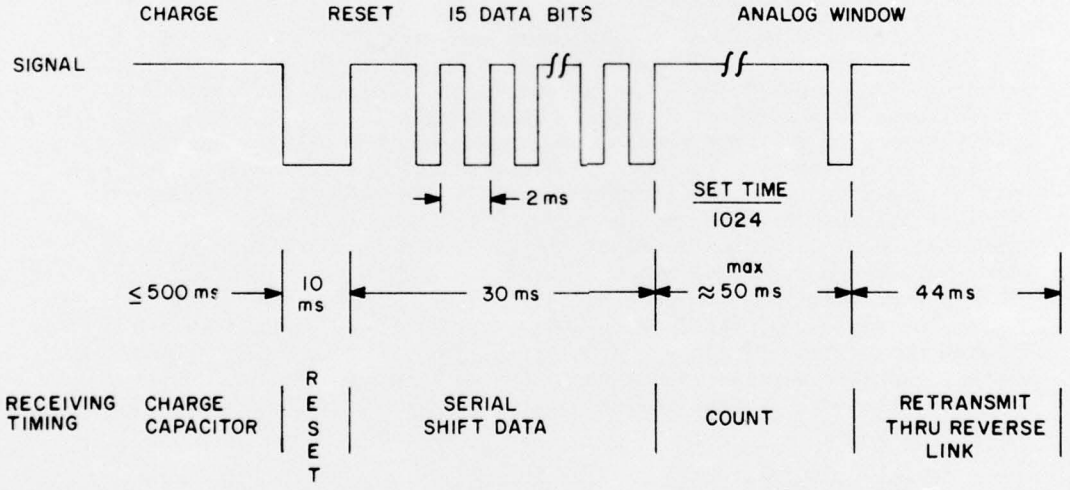

Figure 7. The CMOS memory timing diagram.

DISTRIBUTION

DEFENSE DOCUMENTATION CENTER
CAMERON STATION, BUILDING 5
ALEXANDRIA, VA 22314
ATTN DDC-TCA (12 COPIES)

COMMANDER
USA RSCH & STD GP (EUR)
BOX 65
FPO NEW YORK 09510
ATTN LTC JAMES M. KENNEDY, JR.
CHIEF, PHYSICS & MATH BRANCH

COMMANDER
US ARMY MATERIEL DEVELOPMENT
& READINESS COMMAND
5001 EISENHOWER AVENUE
ALEXANDRIA, VA 22333
ATTN DRXAM-TL, HQ TECH LIBRARY

COMMANDER
USA ARMAMENT COMMAND
ROCK ISLAND, IL 61201
ATTN DRSAR-ASF, FUZE DIV
ATTN DRSAR-RDF, SYS DEV DIV - FUZES

COMMANDER
USA MISSILE & MUNITIONS CENTER & SCHOOL
REDSTONE ARSENAL, AL 35809
ATTN ATSK-CTD-F

COMMANDER
USA MISSILE COMMAND
REDSTONE ARSENAL, AL 35809
ATTN DRSMI-RFGB, G. SULLIVAN

COMMANDER
NAVAL SURFACE WEAPONS CENTER
DAHLGREN, VA 22448
ATTN DG-46, A. KRAMER

COMMANDER
NAVAL SURFACE WEAPONS CENTER
WHITE OAK LABORATORY
SILVER SPRING, MD 20910
ATTN WA-32, D. WASMUND

COMMANDER
NAVAL ELECTRONICS SYSTEMS
SECURITY ENGINEERING CENTER
3801 NEBRASKA AVENUE, NW
WASHINGTON, DC 20390
ATTN L. BAGGETT

COMMANDER
NAVAL RESEARCH LABORATORIES
WASHINGTON, DC 20390
ATTN CODE 5709, W. SCHAEFER

HARRY DIAMOND LABORATORIES
ATTN MCGREGOR, THOMAS, COL, COMMANDING
OFFICER/FLYER, I.N./LANDIS, P.E./
SOMMER, H./CONRAD, E.E.
ATTN CARTER, W.W., DR., ACTING TECHNICAL
DIRECTOR/MARCUS, S.M.
ATTN KIMMEL, S., IO
ATTN CHIEF, 0021
ATTN CHIEF, 0022
ATTN CHIEF, LAB 100
ATTN CHIEF, LAB 200
ATTN CHIEF, LAB 300
ATTN CHIEF, LAB 400
ATTN CHIEF, LAB 500
ATTN CHIEF, LAB 600
ATTN CHIEF, DIV 700
ATTN CHIEF, DIV 800
ATTN CHIEF, LAB 900
ATTN CHIEF, LAB 1000
ATTN RECORD COPY, BR 041
ATTN HDL LIBRARY (3 COPIES)
ATTN CHAIRMAN, EDITORIAL COMMITTEE
ATTN CHIEF, 047
ATTN TECH REPORTS, 013
ATTN PATENT LAW BRANCH, 071
ATTN MCLAUGHLIN, P.W., 741
ATTN CHIEF, BR 410
ATTN CHIEF, BR 420
ATTN CHIEF, BR 430
ATTN CHIEF, BR 440
ATTN MANOLATOS, T., 440 (3 COPIES)